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A TRANSFORMERLESS COMMON-GROUND THREE-SWITCH SINGLE-PHASE INVERTER FOR PHOTOVOLTAIC SYSTEMS

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ABSTRACT

There has been an increasing interest in transformer less inverter for grid-tied photovoltaic (PV) system due to low cost, high efficiency, less weight, etc. Therefore, many transformers less topologies have been proposed and verified with real power injection only. A single-phase transformer less inverter for photovoltaic (PV) applications is introduced. The proposed inverter provides common ground between input and output terminals, which results in the elimination of the leakage current in the PV systems. Moreover, the voltage gain of the proposed inverter is higher than that of the single-phase quasi-Z-source and semi-Z-source inverters. Utilizing the film capacitors makes the proposed inverter more reliable and also increases its lifetime. The operation of the proposed inverter is analyzed in detail. Finally, the performance of the proposed inverter is verified through the experimental results both in off-grid and grid-tied operation modes.

I. INTRODUCTION

Transformers less PV grid-connected inverters have the advantages of small volume, light weight, low cost and high efficiency. However, removing the transformer leads to electrical connection between PV panels and utility grid, resulting in common mode (CM) leakage current, which increases grid connected current harmonics, system losses, and even causes safety issues. Therefore, the application of transformer less PV inverters must meet strict safety standards. In recent years, with increasing application of transformer less PV grid-connected inverters, the research of new topologies to suppress leakage current has become a subject of interest in PV grid-connected systems.

The half-bridge-type inverters connect the utility grid neutral point to the midpoint of DC-link capacitors, so the voltage on parasitic capacitor of PV panels remains unchanged, and the leakage current can be suppressed. This type of topology suppresses leakage current by DC/AC decoupling. However, due to the existence of switch junction capacitors, this kind of method cannot completely disconnect the circuit, so there is still leakage current. Although leakage current can be better suppressed by adding neutral point clamp (NPC) structure. It cannot be eliminated completely, and loss and cost will be increased because of extra structure

The common-ground topology is a kind of topology proposed in recent years, which can completely eliminate leakage current. The principle is to directly connect the negative terminal of PV panels to neutral point of the utility grid, which is equivalent to short-circuiting the parasitic capacitor of PV panels. A

common-ground topology based on virtual DC bus structure is proposed. However, the flying capacitor is not charged in negative half cycle, so the output voltage is distorted in negative half period. The topology proposed in has a two-level output voltage, which has high harmonic content. A multilevel common-ground topology is proposed. But the control method of this topology is very complex.

II. EXISTING SYSTEM

PV system technologies, micro inverters attract the attention of researchers, since they contribute to higher energy harvest in shading conditions. Moreover, due to plug-and-play capability of micro inverters, it is easier to expand the solar system. However, the utilization of micro inverters requires several considerations.

Bipolar sinusoidal pulse width modulation (SPWM)

Transformer less symmetrical inductor-based inverters with a full-bridge converter is commonly used. Although the utilization of bipolar sinusoidal pulse width modulation (SPWM) in these full-bridge-based inverters can significantly decrease the leakage current, it produces a considerable electromagnetic interference noise, high total harmonic distortion (THD), and increased switching losses. On the other hand, when unipolar SPWM is applied, the THD and the inductor size can be reduced. However, it leads to the production of high-frequency common mode voltage and leakage current.

Three-switch three-state single-phase Z-source inverters (TSTS-ZSIs)

Three-switch three-state single-phase Z-source inverters (TSTS-ZSIs) with higher voltage gain, while providing common grounding. However, buck–boost-based type of TSTS-ZSIs has rather complicated signal generation and these inverters cannot produce reactive power

DISADVANTAGES

- Large leakage of currents
- It causes safety issues

III. PROPOSED PROCESS EXPLANATION

PHOTOVOLTAIC (PV) POWER GENERATION

Photovoltaic (PV) power generation systems are received more and more attention in recent years. According to the latest report of IEA-PVPS on installed PV power by the end of 2010, the cumulative installed capacity is increased to almost 35 GW, of which the majorities (69%) are installed in Germany and Italy. The cumulative growth in PV capacity is illustrated from which, it can be observed that most of them is grid-connected. Typically, a line frequency transformer is integrated into the grid-connected PV system for the galvanic isolation, dc injection and leakage current suppression. However, the transformer brings in the additional cost and system efficiency reduction.

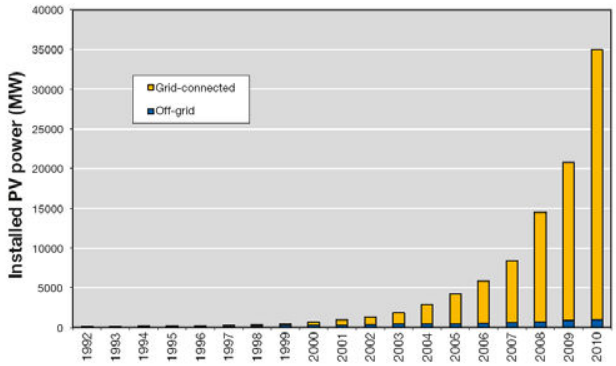

Fig. 1 Cumulative installed capacity between 1992 and 2010 in the IEA-PVPS reporting countries

On the other hand, the transformer less PV systems have been received more attention due to cost and size reduction, as well as efficiency improvement compared with the conventional transformer ones. A number of technical challenges may arise with increased grid-connected transformer less PV systems. However, it leads to the relatively more high frequency ripples due to the two level output voltage. On the other hand, the unipolar modulation with three-level output voltage is beneficial in terms of low voltage ripples and small filter size, but the leakage current is significantly increased due to the time varying high frequency common mode voltage

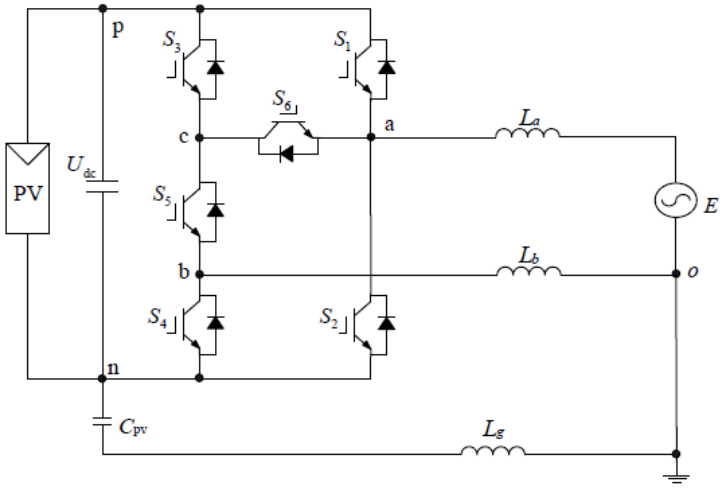

Fig. 2 Schematic diagram of the proposed topology

In order to solve the abovementioned problem, many interesting topologies have been reported in the past few years. The basic idea behind them is to keep the system common mode voltage constant to eliminate the leakage currents. With the basic idea, a new single-phase three level topology for transformer less photovoltaic systems is presented in this paper. Compared with the conventional Hbridge topology, it only needs two additional asymmetrically distributed switches, and the system common-mode voltage can be kept constant with a simple modulation scheme. The theoretical analysis and test results demonstrated that the proposed topology is very promising for transformer less PV systems.

OPERATION PRINCIPLES OF THE PROPOSED INVERTER

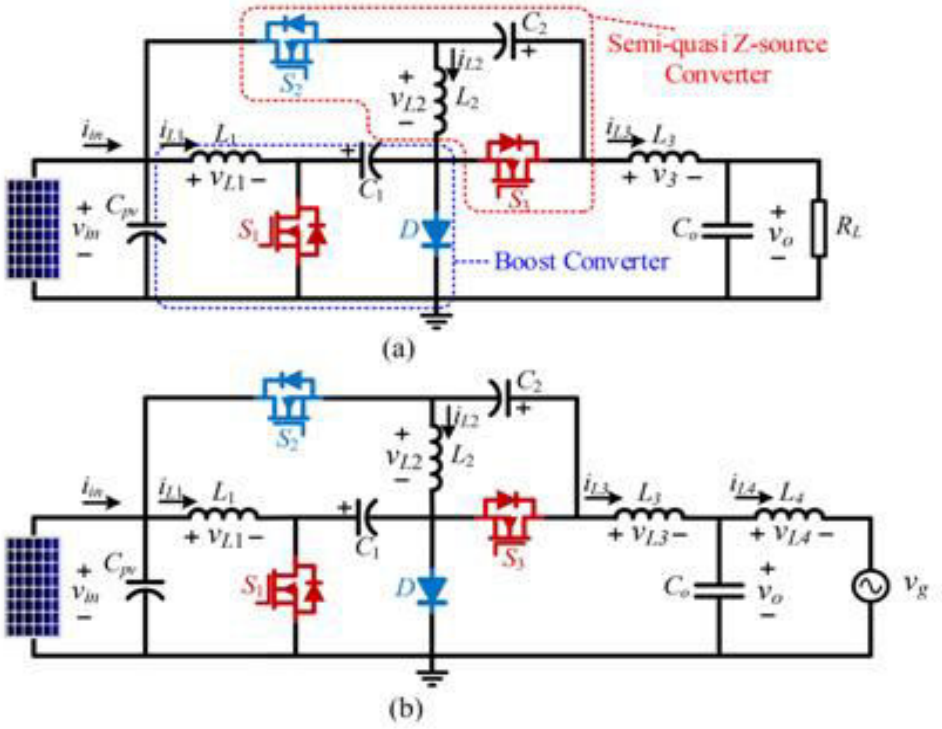

Fig. 3. Proposed inverter (a) in the off-grid mode and (b) in the grid-tied mode

Fig. (a) Shows the proposed inverter in the off-grid mode, including three switches S1, S2, and S3, four capacitors Cpv, C1, C2, and Co, and three inductors L1, L2, and L3. The inductor L3 and the capacitor Co form an LC filter in the output of the inverter. The proposed inverter is composed of one traditional boost converter and one semi-quasi-Z-source topology, as shown in Fig. (a). To facilitate the analysis of the proposed inverter, all components are supposed to be ideal. Moreover, the capacitors are big enough such that their voltages are constant during one switching period.

FULL-BRIDGE THREE PHASE INVERTER

In the case of single-phase PV systems, the output is an ac pulsating signal and in the input side is a smooth dc signal; this system can reach a power rate around 5 kWp. Due this characteristic large dc capacitors are required which can reduce the lifetime and reliability of the system. On the other side, three-phase inverters have at the output a constant ac signal; this means that dc large capacitors are not needed. As an additional characteristic, the total power of the system can be increased, reaching values around 15kWp in the case of rooftop applications. The most widely and simplest topology used in three phase systems is the full-bridge inverter, which consist in three legs, each leg with two transistors (IGBT`s). This topology is commonly used in applications like drivers for ac machines, filter equipments in the electrical grid, etc.

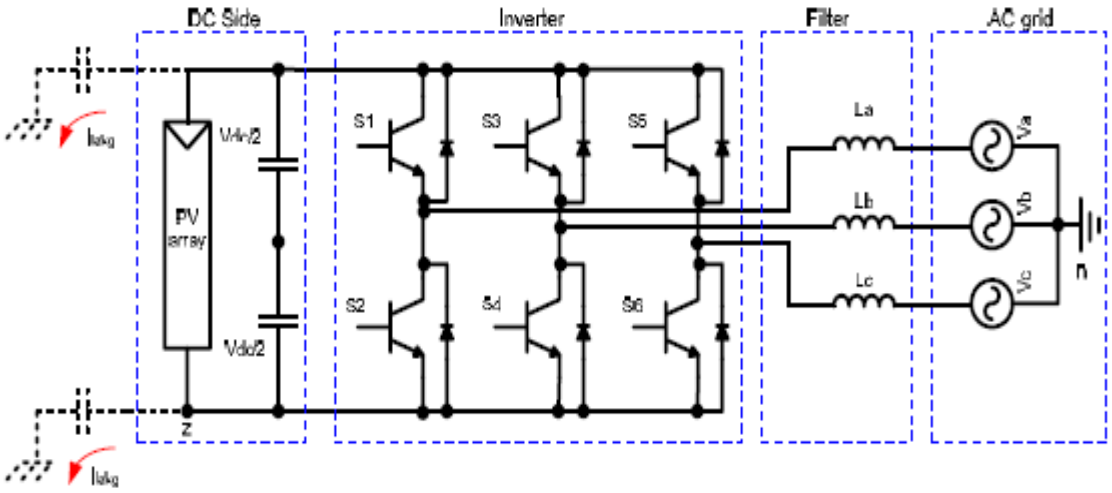

Fig. 4. Three-Phase Full-Bridge Inverter

Therefore, the eight vectors generated by the two-level three-phase inverter can be represented in the same way, as show in Fig

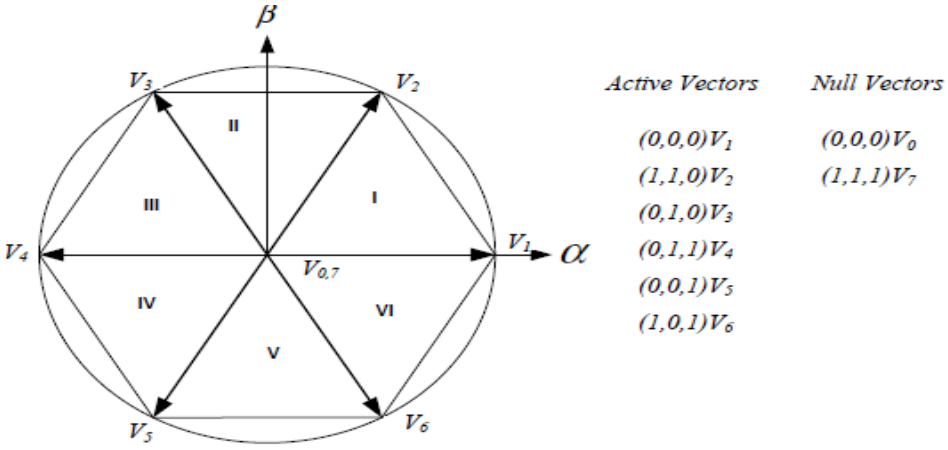

Fig. 5 .General Space Vector Modulation for three-phase inverter

In the standard three-phase two-level inverter shown in Fig the CMV is defining as the average of the sum of voltages between the outputs and a common reference. In this case, the potential between the star point in the load and the "z" common reference for the three outputs, is the CMV which can be expressed by equation

$$V_{nz} = \frac{v_{az} + v_{bz} + v_{cz}}{3}$$

In this way, taking into account the equation (1), it is possible to obtain the common mode voltage generated by each space vector in Fig

Vector	*CMV*
V_0 (0,0,0)	0
V_1 (1,0,0)	1/3 Vdc
V_2 (1,1,0)	2/3 Vdc
V_3 (0,1,0)	1/3 Vdc
V_4 (0,1,1)	2/3 Vdc
V_5 (0,0,1)	1/3 Vdc
V_6 (1,0,1)	2/3 Vdc
V_7 (1,1,1)	+Vdc

Some of these PWM techniques are shown in Fig.

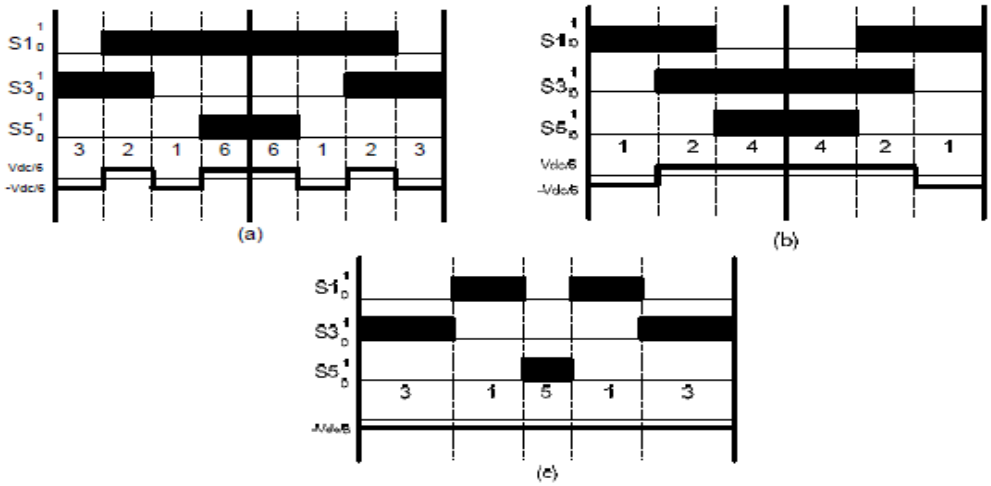

Fig. 6. Reduced Common Mode Voltage Space Vector Modulations

MODE ANALYSIS OF THE PROPOSED INVERTER

Mode I: In this mode, switches S1 and S3 are turned ON, while switch S2 is turned OFF, as depicted in Fig. (a). Inductor L1 is magnetized by the input voltage Vin. Capacitor C2 is charged by inductor L2. Furthermore, C1 is discharged. The equations of this mode can be obtained as

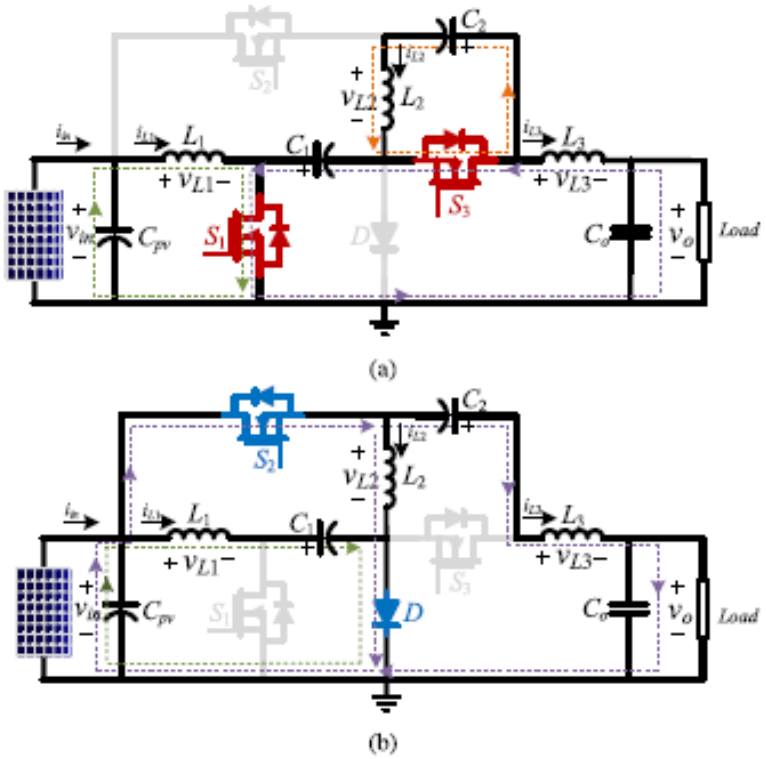

Fig. 7. Operation modes of the proposed inverter. (a) Mode 1. (b) Mode 2.

$$\begin{cases} v_{L1} = v_{\text{in}} \\ v_{L2} = -v_{C2} \\ v_{L3} = -(v_{C1} + v_o) \end{cases} \quad \begin{cases} i_{C1} = i_{L3} \\ i_{C2} = i_{L2} \end{cases}$$

where vL1 , vL2 , vL3 , vC1 , and vC1 denote the voltages across inductorsL1,L2, andL3 and capacitorsC1 andC2, respectively. Vin is the input voltage and Vo depicts the output voltage. Moreover, iC1 , iC2 , iL2 , and iL3 are the currents of capacitors C1 and C2 and inductors L2 and L3, respectively

Mode II: In this mode, according to Fig. (b), switch S2 is turned ON, while switches S1 and S3 are turned OFF. Inductor L1 is charging capacitor C1. Simultaneously, inductor L2 is magnetized by the input voltage Vin. Moreover, capacitor C2 is discharged. The equations of this mode are derived as follows:

$$\begin{cases} v_{L1} = v_{\text{in}} - v_{C1} \\ v_{L2} = v_{\text{in}} \\ v_{L3} = v_{\text{in}} + v_{C2} - v_o \end{cases} \quad \begin{cases} i_{C1} = i_{L1} \\ i_{C2} = -i_{L3} \end{cases}$$

where iL3 is the current of inductor L3.

Nonideal Voltage Gain of the Proposed Inverter

When the parasitic elements of the proposed inverter are considered, the nonideal voltage gain can be written as

$$\frac{V_o}{V_{\text{in}}} = \frac{1-2D}{D(1-D)}\frac{1}{(1-X/R_L)} - \frac{1-2D}{D(1-X/R_L)}\frac{V_D}{V_{\text{in}}}$$

where VD is diode's forward voltage and X is

$$X = -\frac{Dr_{S_1}}{(1-D)^2} - \frac{(1-D)r_{S_2}}{D^2} - \frac{r_{S_3}}{D} - \frac{D^2 r_{L_1}}{(1-D)^2} - r_{L_3} - \frac{(1-D)^2 r_{L_2}}{D^2} - \frac{Dr_{C_1}}{(1-D)} - \frac{(1-D)r_{C_2}}{D} - \frac{(1-2D)^2 r_D}{D^2(1-D)}$$

where $rL1$, $rL2$, and $rL3$ denote inductors' equivalent resistance, $rS2$, $rS2$, and $rS2$ are switches' static drain-to-source ON resistance, and rD is the ON resistance of the diode. If the parasitic elements and the diode's forward voltage are ignored, the value of X will be equal to zero, and therefore, (6) is the same as the ideal gain

Modulation Scheme of the Proposed Inverter

The output voltage and the modulation index are supposed to be

$$v_o = V_m \sin(\omega t)$$

$$M = \frac{V_m}{V_{\text{in}}}$$

where ω, Vm, and M are the angular frequency, the output peak voltage, and the modulation index, respectively. By substituting the following equation can be obtained:

$$D = \frac{2 + M\sin(\omega t) - \sqrt{M^2\sin^2(\omega t) + 4}}{2M\sin(\omega t)}.$$

Fig indicates the gate signal generation scheme, in which a reference signal, namely Vref with an equation equal to is compared to a carrier signal. As can be seen from Fig.Vref is the control signal, which plays the role of the duty cycle and $M\sin(\omega t)$ comes from the controller. $S1$ and $S3$ are conducting when Vref is higher than the carrier, while $S2$ is turned ON when the carrier is higher than Vref. By applying this procedure, a sinusoidal waveform will be generated at the output terminal.

Control of the Proposed Inverter

Control block diagrams of the proposed inverter both in off-grid and grid-tied modes are illustrated. A proportional–resonant (PR2) controller is utilized in the control loop, which produces a sinusoidal signal,

Msin(ωt), as an input for (10). The resultant varying duty cycle is then compared with the carrier signal to generate the switch pulses. The phase of the output current of the inverter comes from the phase-locked loop (PLL) unit. The generated reference signal of the output current is used to control the output current through PR1 similar to Fig.

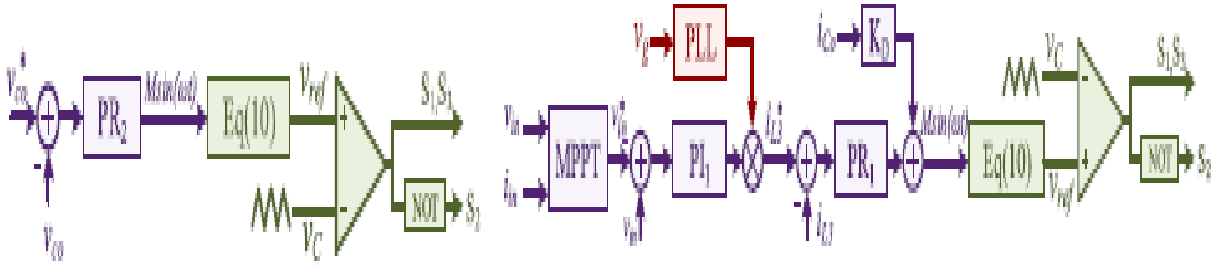

Fig 8. Control Block diagram

The equations of PI and PR controllers are as follows:

$$\mathrm{PI}(s) = K_P + \frac{K_I}{s}$$

$$\mathrm{PR}(s) = K_P + \frac{K_R.s}{s^2 + K_C.s + \omega^2}$$

In this method, a signal that comes from the output capacitor current *iCo* with a gain of *KD* is added to the output of the current controller, PR1. It is worth mentioning that every MPPT technique can be adopted into this control system.

FLYING CAPACITOR SELECTION

The main idea of proposed topology is to charge the flying capacitor at the positive half period of grid voltage and to supply the power by the flying capacitor at the negative half period. Therefore, the choice of flying capacitor is very important for proposed topology. During a switching cycle, there are three modes of flying capacitor charging and one mode of discharging. The energy released by the capacitor is approximately equal to the energy absorbed by the unity grid. A model can be built, as shown in

$$\frac{1}{2}C(u_1^2 - u_2^2) = \int_{t_1}^{t_1+\Delta t} u_g i_g dt$$

$$t_1 \in (0.01 + 0.02k, 0.02 + 0.02k), \quad k \in N$$

where u1 and u2 are voltage of flying capacitor, ug and ig are the voltage and current of the unity grid.

$$u_g = U_g \sin(\omega t)$$
$$i_g = I_g \sin(\omega t)$$
$$\Delta t = \frac{1}{4} \times \frac{1}{f_{sw}}$$

QZSI OPERATION AND MODULATION

The traditional three-phase VSI shown utilizes eight different switching states in order to modulate the B6-bridge and to achieve the inversion operation. These eight states comprises six active states and two zero states. In addition to these different eight switching states, the three phase qZSI shown in Fig can utilize an additional switching state, which is not permissible in the traditional VSIs, in order to embrace the boosting capability within the inversion operation. This additional switching state, which is called ST state, is permissible in the impedance source inverters due to the utilization of an impedance network between the dc source and the B6-bridge as depicted

Then, according to the value of the impedance network inductors, using the SBMSV modulation scheme, can be calculated by

$$L_{n1} = L_{n2} = L_n \geq \frac{M \cdot (1 - M) \cdot V_{in}}{(2M - 1) \cdot f_s \cdot \Delta I_L},$$

where M is the modulation index defined in Fig. 4, Vin is the input dc voltage, fs is the switching frequency, and ΔIL is the peak-to-peak inductor current ripple. Hence, assuming that the input power is equal to the output power, Ln can be calculated for the rated output power (Po) from

$$L_n \geq \frac{M \cdot (1 - M) \cdot P_o}{(2M - 1) \cdot f_s \cdot \Delta I_L \cdot I_{in}},$$

where Iin is the average input current. Thus, considering a certain desired peak-to-peak inductor current ripple (ΔIL) at full-load, the required impedance network inductance (Ln) can be calculated

Operation of qZS-CMI

Figure shows the topology of quasi-Z-source inverter. Quasi-Z-source inverter has two modes of operation at the DC side: the non-shoot-through state (active state and conventional zero state) and shoot-through state. The unique LC and diode network connected to the inverter bridge modify the operation of the circuit, allowing shoot through state

Active or Non-shoot-Through State

In the non-shoot-through state, the inverter bridge is equivalent to the current source. Considering T as the interval of one switching cycle, interval of shoot-through state is T0; the interval of non-shoot-through state is T1; thus, T = T0 ? T1; and shoot-through duty ratio, D = T0/ T1. The equations corresponding to non-shoot-through state are given as,

$$v_{L1} = V_{in} - V_{C1}$$

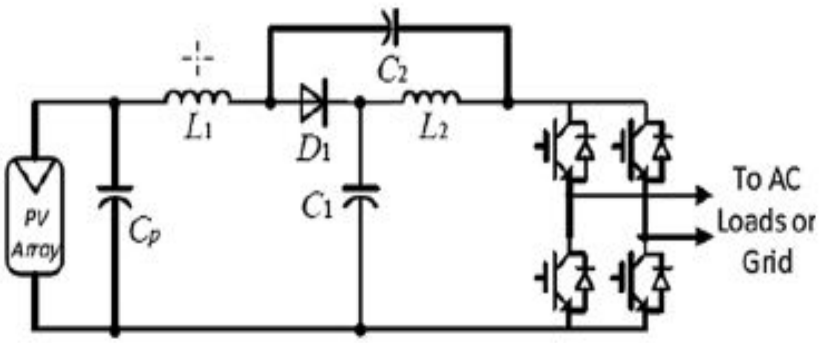

Fig. 9 Quasi-Z-source inverter

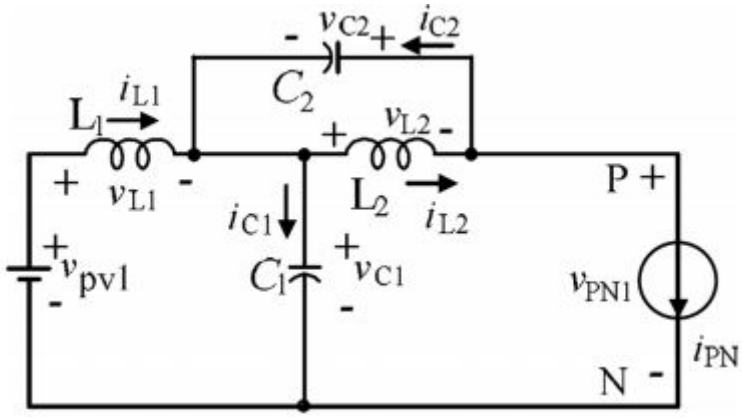

Fig. 10 Equivalent circuit of qZSI—non-shoot-through state

$$v_{L2} = -V_{C2}$$
$$v_{PN} = V_{C1} - v_{L2} = V_{C1} + V_{C2}$$
$$v_{diode} = 0$$

where VC1 and VC2 are the capacitor voltages and VL1 and VL2 are the inductor voltages of the impedance network.

Shoot-Through State

In shoot-through state, both the switches of at least one leg will conduct simultaneously. This state is forbidden in the traditional VSI, because it will cause short circuit of the voltage source and damage the devices. Figure shows the equivalent circuit of qZSI in shoot-through state. The equations corresponding to shoot-through state are given as

$$v_{L1} = V_{in} + V_{C2}$$
$$v_{L2} = V_{C1}$$
$$v_{PN} = 0$$
$$v_{diode} = V_{C1} + V_{C2}$$

At steady state, the average voltage of the inductors over one switching cycle is zero.

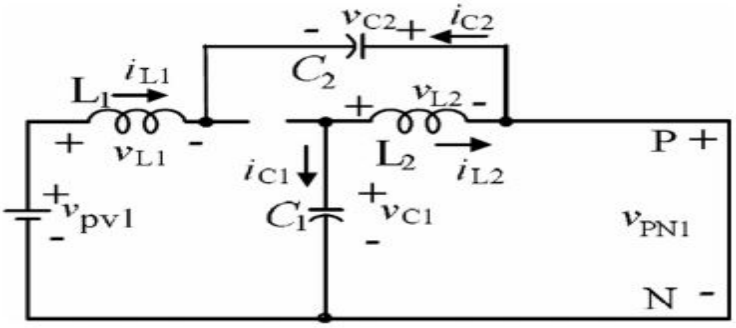

Fig. 11 Equivalent circuit of qZSI—shoot-through state

$$V_{L1} = v_{L1} = \frac{T_0(V_{C2} + V_{in}) + T_1(V_{in} - V_{C1})}{T} = 0$$
$$V_{L2} = v_{L2} = \frac{T_0(V_{C1}) + T_1(V_{C2})}{T} = 0$$

SEMI-Z-SOURCE INVERTER

A single stage transformer less semi-Z-source inverter for grid connected application for renewable energy DGs is presented in this paper. This inverter minimizes common mode leakage current with its ground sharing features, ensures less THD and DC current injections to the grid. This topology has some benefits over traditional Z source inverter topology. It contains Z source network in AC side of the semi-Z-source network which is different from conventional topology and results in size minimization. To generate sinusoidal voltage at the output, the proposed topology uses the nonlinear sinusoidal voltage gain curve as voltage reference.

BASIC PRINCIPLE OF TRANSFORMERLESS SEMI-Z-SOURCE INVERTER

Z-source and quasi-Z-source dc-dc converters are shown in Fig. which has the ground sharing nature. Fig. shows the continuous voltage gain curve of Fig. Topologies shown in Fig. have the ability to produce positive and negative voltage at the output with continuous voltage gain curve. So, within duty cycle from 0 to 2/3 and appropriate modulation strategy, these two topologies can be used as inverter with -Yin to +Yin at the output as like as the traditional full bridge inverter.

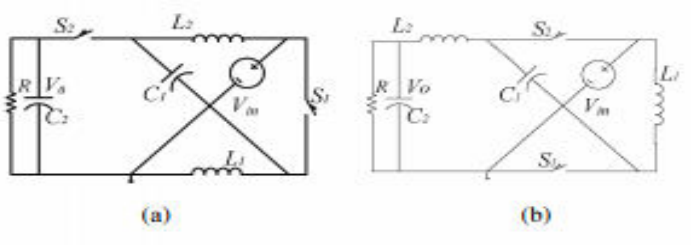

Fig. 12. Z-source and quasi-Z-source dc-dc converters with continuous voltage gain.

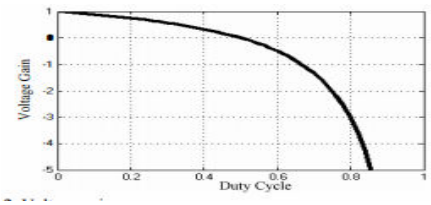

Fig. 13. Voltage gain curve.

The two states of operation respectively. In state I, the switch Sl conducts where input voltage source and capacitor Cj charge the two inductors. For state II, switch S2 conducts and two inductors have turned into sources. The direction of current references of the inductor and the voltage references of the capacitor are shown in the figure for the following steady state equations. A detail of the modes of DC operation is shown. Based on inductor voltage second balance and capacitor charge balance principle, the steady state equations are as follows;

$$\frac{V_o}{V_{in}} = \frac{1-2D}{1-D}$$

$$V_{C1} = \frac{D}{1-D} V_{in}$$

$$I_{L2} = -I_o$$

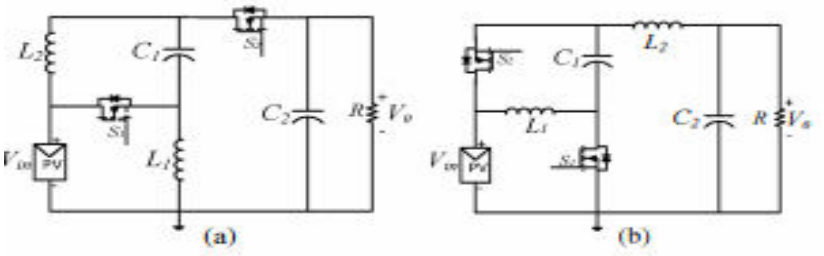

Fig. 14. Single phase semi-Z-source inverters.

Space Vector Pulse Width Modulation (SV-PWM)

SVPWM is the best computational PWM technique for a three phase voltage source inverter because of it provides less THD & better PF. SVPWM works on the principle that when upper transistor is switched ON; corresponding lower transistor is switched OFF. The ON and OFF state of the upper switches (S1, S3, S5) evaluates the output voltages. This section briefly discusses the space vector PWM principle. This PWM

method is frequently used in vector controlled and direct torque controlled drives. In vector controlled drive this technique is used for reference voltage generation when current control is exercised in rotating reference frame.

It is seen in the previous section that a three-phase VSI generates eight switching states which include six active and two zero states. These vectors form a hexagon (Fig. 3) which can be seen as consisting of six sectors spanning 60° each. The reference vector which represents three-phase sinusoidal voltage is generated using SVPWM by switching between two nearest active vectors and zero vectors

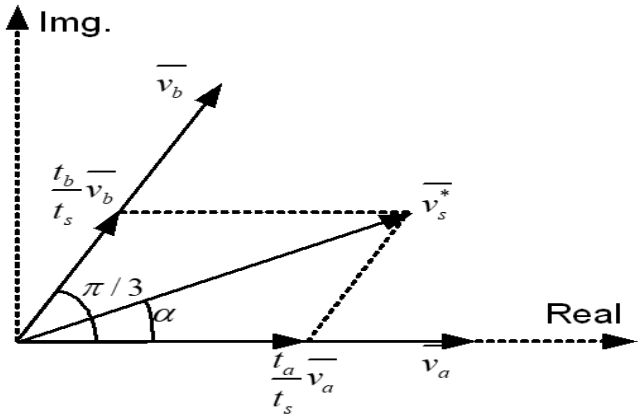

Fig 15 principle of space vector time calculation

IV. TEST RESULT AND ANALYSIS

TESTING

A program represents the logical elements of a system. For a program to run satisfactorily, it must compile and test data correctly and tie in properly with other programs. Achieving an error-free program is the responsibility of the programmer. Program testing checks for two types of errors: syntax and logic.

Software testing is an important element of software quality assurance and represents the ultimate review of specification, design and loading. The increasing visibility of software AR a system element and the costs associated with a software failure are motivating for well planned through testing.

TEST OBJECTIVES

These are several rules that can save as testing objectives they are: Testing is a process of executing program with the intent of finding an error. A good test case is one that has a high probability of finding an undiscovered error. If testing is conducted successfully according to the objectives as stated above it would in cover errors in the software also testing demonstrator that software functions appear to the working according to specification that performance requirements appear to have been met.

PROGRAM TESTING

There are three ways to test a program

1. for correctness
2. For implementation, efficiency and
3. For Computations complex city.

Test for correctness is supposed to verify that a program does actually what it is designed to do. This is much more difficult than it May appear at first, especially for large programs. Test for implementation efficiency attempt to find ways to make a correct program faster or use less storage.

TEST CASES

System testing is testing conducted on a complete, integrated system to evaluate the system's compliance with its specified requirements. System testing falls within the scope of black box testing, and as such, should require no knowledge of the inner design of the code or logic.In unit testing, the entire program that makes the system tested. Unit testing first focuses on the modules, independent of one another to locate errors. This enables to detect errors in coding and the logic within the module alone. In the unit testing control path are tested to remove errors within the boundary of the module.

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